NOV 2 2 2005

#### IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application Serial No	09/292,132
Filing Date	April 14, 1999
Inventor	Salman Akram et al.
Assignee	Micron Technology, Inc.
Group Art Unit	
Examiner	Savitri Malpuri
Customer No	021567
Attorney Docket No	
Title: Methods of Forming a Transistor Gate	

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

### **CERTIFICATE OF FACSIMILE TRANSMISSION UNDER 37 CFR § 1.8**

I hereby certify that the following papers are being facsimile transmitted to the Patent and Trademark Office at (571) 273-8300 on the date shown below:

- 1. Certificate of Facsimile Transmission
- 2. Examiner Interview Summary

ted:  $\frac{MQQ/OS}{}$  By:

Julie A. Foster

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NUMBER OF PAGES IN FACSIMILE: 2

#### **FEE DEFICIENCY**

Although it is believed that no fees are due, the Commissioner is hereby authorized to charge any fees under 37 C.F.R. 1.16 and 1.17 which may be required by this paper to Deposit Account No. 23-0925.

Application Serial No. 09/292,132
Examiner Interview Summary of November 22, 2005

NOV 2 2 2005

MI22-1171

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No.	
Filing Date	April 14, 1999
Inventor	Salman Akram et al.
Assignee	Micron Technology, Inc.
Group Art Unit	2812
Examiner	Savitri Mulpuri
Attorney's Docket No	MI22-1171
Customer No	021567
Title: Methods of Forming a Transistor Gate	

Title: Methods of Forming a Transistor Gate

# **EXAMINER INTERVIEW SUMMARY OF NOVEMBER 22, 2005**

To:

**Commissioner for Patents** 

P.O. Box 1450

Alexandria, VA 22313-1450

From:

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Applicant's representative held an interview with Examiner Mulpuri on November 22, 2005. Applicant's representative would like to thank Examiner Mulpuri for her time and attention to this matter.

The pending rejection under 35 U.S. §112, first paragraph, against claims 88, 90 and 99-101 were discussed. No agreement was reached.

Respectfully submitted,

Dated: 11-22-05

Rv

y:

D. Brent Kenady Reg. No. 40,045